Amendments to the Specification:

Please replace paragraph **[01]** with the following amended paragraph:

[01] This application is related to commonly-assigned, co-pending U.S. patent application number[s 09/___,___, filed _____, (Attorney Docket No. 15114-054510US/A718), entitled "Enhanced DQS Clock Architecture with Precise Phase Shift Control," by Huang et al., and 09/___,___]10/037,861, filed [_____]January 12, 2002 (Attorney Docket No. 015114-054810US/A721), entitled "Self-Compensating Delay Chain for Multiple Data-Rate Interfaces," by Chong et al., [both of]which [are]is hereby incorporated by reference in [their]its entirety.

Please replace paragraphs **[15]** and **[16]** with the following amended paragraphs:

[15] Figure 5 is a block diagram of the internal circuitry of a PLD according to an exemplary embodiment of the present invention; [and]

[16] Figure 6 is a block diagram of an exemplary computing system that employs a multiple-data-rate PLD according to an embodiment of the present invention; and

Please insert the following new paragraph after present paragraph **[16]**:

[16.1] Figure 7 shows an exemplary implementation for a phase control circuit according to an embodiment of the present invention.

Please replace paragraphs **[17]** and **[18]** with the following amended paragraphs:

[17] To minimize skew, accommodate a wide frequency range of operation, and facilitate rapid pin migration to larger PLDs, the present invention provides a modular multiple-data-rate I/O architecture that can be readily replicated and scaled. For illustrative purposes, the invention is described in the context of a double-data rate

(DDR) system. It is to be understood, however, that the principles of this invention can be applied to systems operating at quad-data rate or higher. Referring to Figure 2, there is shown a block diagram of an I/O module 200 for a PLD configured for DDR operation according to one embodiment of the present invention. In this embodiment, DDR interface module 200 includes a number of, in this example eight, data I/O cells each having a data I/O pin DQ and a DDR register block 202 made up of a pair of data registers R1 and R2. Module 200 also includes a strobe input cell which is preferably located at a central location vis [a]á vis other I/O cells, and includes a strobe signal pin DQS and phase delay circuit 204. Phase delay circuit 204 causes a 90 degree phase shift in the input strobe signal DQS and applies the phase shifted strobe signal to the module clock net 206 that is a local clock line dedicated to the I/O [registers]cells inside module 200. Local clock net 206 has programmable connection to drive all input registers of [DQs]register blocks 202 in the DDR interface group. Thus, this DDR clock scheme allows for maintaining the clock skew between DQ and DQS to remain within a controllable range. The overall PLD I/O architecture includes multiple modules 200 each of which has its own DQS resources (DQS pin, phase shift circuit 204, and local clock net 206).

[18] Phase shift circuit 204 is a programmably controlled delay chain that adjusts its delay in response to phase control signal PC. Phase control signal PC is a multi-bit (e.g., 6 bit) binary signal that is supplied by a master phase control circuit 208. Master phase control circuit 208 operates in response to a system clock arriving at any one of multiple clock pins 210, and is shared by a number of modules 200. In one embodiment, master phase control circuit 208 is a delay-locked loop (DLL) that takes into account the PLD operating frequency, PVT variations as well as contributions by other potential sources of delay to generate control signal PC to achieve the desired 90 degree phase shift locally in the various DDR I/O modules 200. Various embodiments for master control circuit 208 and phase shift circuit 204 are described in greater detail in the above-referenced commonly-assigned, co-pending patent application number

[09/___,___, (Atty Dkt No. 015114-054510US/A718 titled "Enhanced DQS Clock Architecture with Precise Phase Shift Control]10/037,861, filed January 12, 2002 (Attorney Docket No. 015114-054810US/A721), entitled "Self-Compensating Delay Chain for Multiple Data-Rate Interfaces," by Chong et al. One example for an implementation of the control circuit 208 is shown in Figure 7. Referring to Figure 7, control circuit 700 includes frequency dividers 706 and 780, variable-delay buffers 710, 720, 730, and 740, phase detector 750, flip-flop 751, up/down counter 760, and inverter 790. The up/down counter may be a binarily-weighted, thermal, or other type of up/down counter, such as a combination binarily-weighted and thermal counter. In a specific embodiment, the counter is binarily weighted.

Please add the following paragraphs after paragraph **[18]**:

[18.1] A system clock signal on line 705 is received by frequency divider 706. Frequency divider 706 divides the system clock signal's frequency, thereby generating the CLKIN signal on line 707. In a specific embodiment, frequency divider 706 divides the system clock frequency by 8. Alternately, other frequency divisions are possible, such a divide by 4, 16, or other value. The lower frequency CLKIN signal on line 707 is delayed by variable-delay buffers 710, 720, 730, and 740. A delayed clock signal on line 745 is provided to phase detector 750. Delay match element 770 is designed to match the delay in the frequency divider 706, and provide an output signal on line 775 to the phase detector 750. The phase detector 750 determines the phase relationship between the system clock and the delayed clock, for example, whether a rising edge of the system clock precedes a rising edge of the delayed clock. Alternately, the phase detector may determine whether a falling edge of the system clock precedes a falling edge of the delayed clock.

[18.2] In a specific embodiment, phase detector 750 does this by determining the level of the delayed clock signal on line 745 at the rising edges of the clock signal on line 775. This level detection results in output signal Q1 on line 777, which is input to flip-

flop 751. Flip-flop 751 is clocked by the system clock on line 705 and provides the up/down signal 755 to the up/down counter 760. A second frequency divider 780 divides the system clock's frequency, thus generating signal NCONTCLK on line 785. Again, in a specific embodiment of the present invention, frequency divider 780 divides the system clock frequency by eight. In other embodiments, this divisor may be different, such as 4, 16, or other appropriate value. The NCONTCLK signal on line 785 is inverted by inverter 790, resulting in a CONTCLK signal on line 795. The CONTCLK signal on line 795 clocks the up/down signal on line 755 into the up/down counter, resulting in the output signal Ct[5:0] on bus 765.

[18.3] Again, when the output of up/down counter 760 changes, the delays through the variable-delay buffers 710 through 740 change. But this change in delay is not instantaneous, and takes a finite duration to reach a final value. In a specific embodiment, frequency dividers 706 and 780 are separate frequency dividers such that their output edges may be timed to give the variable-delay buffers 710 through 740 a maximum duration in which to settle. In other embodiments, frequency dividers 706 and 780 may be the same frequency divider.

[18.4] Again, the delay match element 770 is designed to match the delay between a system clock rising edge and a CLKIN rising edge on lines 705 and 707. Matching these delays enables the phase detector 750 to adjust the delay of the variable-delay buffers 710 through 740 with a minimum amount of systematic delay errors.

[18.5] The variable-delay buffers 710 through 740 match or are similar to the variable-delay buffer 120 in Figure 1. The cumulative delay provided by variable-delay buffers 710-740 is one clock cycle or 360 degrees. In a double-data-rate interface the delay of the variable-delay buffer 120 in Figure 1 is one-fourth the cumulative delay of the variable-delay buffers 710 through 740, or one-quarter of a clock cycle or 90 degrees. In other multiple-data-rate interfaces the phase shift may be different, and there may be more variable-delay buffers like 120 in Figure 1 providing different delays. For example,

delays of 60 and 120, or 45, 90, and 135 degrees may be provided by multiple variable-delay buffers connected in series or parallel. These delays can be used in triple and quadruple-data-rate interfaces, respectively. Alternately, they may be used in other data-rate interfaces.

[18.6] In other embodiments, the system clock and DQS signal may be harmonics or have frequencies that are multiple of each other. For example, the DQS signal may be the second harmonic, or have twice the frequency of the system clock. In that case, a delay of one system clock cycle in the divided system clock signal CLKIN corresponds to a two cycle delay in the DQS signal. Accordingly, eight elements may be used in the system clock delay path, while one matching element is used in the DQS path.

[18.7] One skilled in the relevant art appreciates that this block diagram may be drawn differently without deviating from the scope of the present invention. For example, the phase detector 750 and flip-flop 751 may be considered as a single phase detector block. Also, the flip-flop 751 may be considered as a block inside the up/down counter 760. Further, the variable-delay buffers 710 through 740 may be in front of the frequency divider 706, or some of the variable-delay buffers 710 through 740 may be in front of the frequency divider 706, while the remainder follow it.

Please replace paragraphs **[19]**, **[20]** and **[21]**with the following amended paragraphs:

[19] Referring back to Figure 2, it [It] is to be understood that module 200 is a specific example described herein for illustrative purposes only. Many different variations and alternatives are possible. For example, the number of I/O cells in each module 200 may vary depending on the application. In some embodiments, a module 200 may include non-DDR I/O registers. That is, a DDR interface module 200 may include, for example, eight DDR register blocks 202 plus several additional general-purpose I/O registers to add further flexibility. In a variation of this embodiment where all I/O cells and the strobe input cell are designed identically, any eight cells within the

module can be selected to be DDR DQ cells, while the cell that is as close to the center as possible would be selected as the DQS cell. In this embodiment, the DQS cells that include data registers can be used as other normal data registers in non-DDR applications. In such an embodiment, the DQS cell can be programmably configured to have the DQS pin connect to phase shift circuit 204 (in case of a DDR application), or alternatively to normal I/O registers (in case of non-DDR application). In applications with higher data rates (e.g., quad data rate), module 200 may include more than one DQS cell, and DDR register blocks 202 may include more than two (e.g., four) registers.

[20] Another advantage of the multiple-data-rate interface architecture for a PLD according to the present invention is that it allows the I/O structure to be easily scaled to a higher pin count for larger PLDs. Figure 3 shows the I/O bank along one edge of a PLD die for two devices, 300 and 302. In this example, PLD 300 represents the smallest device in a PLD product family and PLD 302 is the largest. Both I/O banks of PLD 300 and PLD 302 are partitioned into a fixed number, e.g., 10, of DDR I/O sections 304-0 to 304-9. An exemplary embodiment for the internal resources of a DDR I/O section 304 is shown in Figure 2. In any given PLD, each I/O section 304 includes the same number of I/O cells, e.g., 10, while for different PLDs this number will vary up to, e.g., 35. Regardless of the size of the PLD, however, each DDR I/O section 304 forms a single DDR interface module with independent DQS resources. That is, each DDR I/O section 304, whether in the smallest device in the family or the largest, includes at least one DQS pin and its associated circuitry, multiple, e.g., eight DQ[s] pins and DQ registers, and one local clock net as shown, for example, in Figure 2. Once again, those skilled in the art will appreciate that the I/O bank according to the present invention need not necessarily include 10 DDR I/O sections 304, and may instead include fewer or larger number of sections.

[21] The flexibility afforded by the I/O architecture of the present invention speeds up the time-to-market cycle for new and larger PLDs. When designing a next

generation PLD, because of the uncertainty regarding the eventual die size as well as the package hardware restrictions, the designer is unable to decide on the location of DQ and DQS pins until the end of the design cycle. This adds further delays to the design cycle. The present invention essentially eliminates this delay by providing a modular I/O architecture that [is] can be easily scaled such that the boundaries of each I/O section can still be defined at an early design stage. According to one embodiment of the invention, the DDR I/O section may have a number of I/O registers that is larger than the minimum (e.g., 8) required for a particular multiple-data-rate (e.g., DDR) system. With pre-defined boundaries, however, the sections can be placed while final DQS locations can be decided at a later time from one of multiple possible pins in the DDR I/O section followed by the DQ and local clock net. [Philip, assuming this requires ALL I/O cells to be identical in resources, does that mean that each one is equipped with the phase delay circuit also? If not, how can the designer select the DQS pin to be any among the whole section?]